Doc Code: AP.PRE.REQ

PTO/SB/33 (07-05)
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
EFIM0252

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on .....

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Typed or printed name .....

Application Number	Filed
09/521,280	07-Mar-2000

First Named Inventor: Stephan Voges

Art Unit	Examiner
2192	ERIC B. KISS

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [x] attorney or agent of record. Registration number 39,862
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 .....

/James Trosino/
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23-Feb-2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

- [x] *Total of 1 forms are submitted.

ATTORNEY DOCKET NO. EFIM0252

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Stephen Voges et al.
Application No.	:	09/521,280
Filed	:	07 March 2000
For	:	METHODS AND APPARATUS FOR HARDWARE SIMULATION AND DESIGN VERIFICATION
Group Art Unit	:	2192
Examiner	:	ERIC B. KISS

Mail Stop AF
Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

STATEMENT IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Claims 1, 5, 57 and 59 are currently pending. All of the pending claims have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite because the claims include the trademark/trade name "VERILOG." In addition, claims 1, 5, 57 and 59 have been rejected under 35 U.S.C. §102(b) as being anticipated by Joe LoCicero and Donald E. Thomas, "A Multithreaded Multiple-Language Hardware/Software Cosimulator," 1997, Carnegie Mellon University, Research Report No. CMUCAD-97-34 ("LoC1997").

Applicants respectfully submit that these rejections are clearly erroneous. In particular, the Examiner has failed to establish that the pending claims are indefinite, and has erroneously concluded that the claims include a trademark used to identify or describe a particular material or product. In addition, the Examiner has failed to establish a prima facie case of anticipation. Indeed, LoC1997 does not include specific claim limitations, and actually points away from the claimed invention. Applicants

respectfully request that this Request be granted, and that the Examiner's rejections be withdrawn.

The § 112, Second Paragraph Rejection is Clearly Erroneous

The 22 November 2006 Final Office action (the "Final Action") has asserted that all of the pending claims are indefinite because the claims include the trademark "VERILOG." In particular, the Final Action at 2 states that "the trademark VERILOG is used to describe a particular simulation environment." Applicants respectfully disagree.

The MPEP states that "the presence of a trademark or trade name in a claim is not, per se, improper under 35 U.S.C. 112, second paragraph, but the claim should be carefully analyzed to determine how the mark or name is used in the claim. It is important to recognize that a trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name . . . . If the trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of the [sic] 35 U.S.C. 112, second paragraph."

The term "VERILOG" is not used in any of the pending claims to identify or describe a particular material or product. In particular, a person of ordinary skill in the art would understand the term "VERILOG simulator" is not used in the application or the claims to identify or describe any specific VERILOG simulator (of which there are many), but instead is used to refer to any simulator that runs VERILOG code. Accordingly, because the claim terms are not indefinite, applicants respectfully request that the § 112, second paragraph rejections be withdrawn.

The § 102(b) Rejection is Clearly Erroneous

Independent claims 1 and 59 recite methods for providing a design test bench, the methods including, among other things, providing a single executable program adapted to create a primary thread and a secondary thread, the primary thread running VERILOG code on a VERILOG simulator, the secondary thread running an interpreter that interprets a scripted routine comprising a user-defined call that is mapped to a VERILOG task. As previously stated, LoC1997 does not describe the

claimed invention, but instead describes a "cosimulator" environment in which VERILOG code is converted to "an internal, stylized form of C++," and then the converted code is compiled and linked with C++ functions to form a completed simulation environment. (Page 6; FIG. 1). In this regard, LoC1997 describes a system that implements its own unique (non-VERILOG) simulator that runs C++ code.

The Examiner has failed to establish a prima facie case of anticipation because LoC1997 does not describe methods that include providing a single executable program adapted to create a primary thread running VERILOG code on a VERILOG simulator. In this regard, the Examiner has not only ignored the actual claim language, but also has mischaracterized applicants' arguments. In particular, the Final Action at 3 states: "Applicant contends that LoC1997 fails to disclose a primary thread running VERILOG code on a VERILOG simulator. (Remarks (9/12/2006) at p.4). This contention is unfounded." Contrary to the Examiner's assertion, applicants have consistently argued that the claims require providing a single executable program adapted to create a primary thread running VERILOG code on a VERILOG simulator. See, e.g., Reply to 6 September 2006 Office action at 4; Reply to 19 May 2006 Final Office action at 5.

Ignoring applicants' actual argument (and the actual claim language), the Examiner additionally asserts that "the internal conversion of VERILOG code does not change the fact that the LoCicero system simulates VERILOG code. . . . VERILOG code goes in, and simulation results come out. . . . It is clear from the disclosure of LoCicero . . . [that] the simulation engine of LoCicero may be considered a VERILOG simulator." (Final Action at 3-4). Applicants respectfully submit that these assertions are irrelevant, and have nothing to do with the actual claim language in this application. Indeed, the claims do not merely recite a method of "simulating VERILOG code," or providing a "VERILOG simulator."

Instead, the claims require providing a single executable program adapted to create a primary thread and one or more secondary threads, the primary thread running VERILOG code on a VERILOG simulator. LoC1997 does not describe or suggest such a step, and instead expressly points away from it by describing a system that implements a simulator that runs C++ code, not VERILOG code. Because the Examiner has failed to establish a prima facie case of anticipation, applicants respectfully request that the § 102(b) rejections be withdrawn.

Applicants should not be required to incur the time and additional expense of preparing and filing an appeal brief, and further prosecuting an appeal of the clearly erroneous rejections in this case. Accordingly, applicants respectfully request that this Request be granted, and that the Examiner's rejections be withdrawn.

Respectfully submitted,

/James Trosino/
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